DETAILED ACTION

1. This Office Action incorporates an Examiner's Amendment, a Rejoinder, and Reasons For Allowance.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/02/2008 has been entered.

3. The Applicant's response to the last Office Action, filed 10/10/2008 has also been entered and made of record.

4. The Applicant has included newly added claim(s) 49.

5. The application has pending claim(s) 1 and 3-49.

6. In response to the Request for Continued Examination filed on 9/02/2008 and the Supplemental Amendment filed 10/10/2008:

The "Claim rejections under 35 U.S.C. 112, second paragraph" have been entered and therefore the Examiner withdraws the rejections under 35 U.S.C. 112, second paragraph.

EXAMINER'S AMENDMENT

7. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ameya Purohit and John Castellano on December 23, 2008.

The application has been amended as follows:

For the claims on pages 2-17 of the Applicant's Supplemental Amendment dated 10/10/2008:

1. Please further amend claims 1, 32, and 49 as shown by the attached pages.

Claim 1: (Currently Amended) An image processing apparatus for converting image data between a raster scan order and a block scan order, comprising:

an image data processor for supplying image data of a raster scan order having a given horizontal resolution and a given vertical resolution;

a line memory for storing image data of a plurality of lines;

an address generating block for converting supplied image data of raster scan order to block scan order by generating a common read/write address for the line memory so that only one line memory is required for performing simultaneous read and write operations, the address generating block including

a block address generator for generating an address of a block which image data is read from and written into;

a line offset generator for providing a line offset between an earlier common read/write address and a present common read/write address for the line memory; and

an address generator including ~~a multiplexer, a next anchor address register, a anchor address register, a common read/write address operator and at least two adders, for generating the common read/write address for the line memory based on the block address and the line offset~~

a multiplexer sequentially providing a plurality of input values including at least one output of at least two adders and the address of the block to a next anchor address register;

a first adder of the at least two adders outputting a sum of a next anchor address of the next anchor address register and the line offset;

a second adder of the at least two adders outputting a difference of the next anchor address of the next anchor address register and a desired value;

an anchor address register receiving the next anchor address from the next anchor address register; and

a common read/write address operator operating upon the received next anchor address to generate the common read/write address; and

an encoder receiving image data of the block scan order from the line memory and encoding the received image data.

Claim 32: (Currently Amended) A method for converting image data between a raster scan order and a block scan order, comprising

receiving image data of a raster scan order having a given horizontal resolution and a given vertical resolution;

generating a common read/write address for a line memory of a plurality of lines for performing simultaneous read and write operations using an address generator having ~~a multiplexer, a next anchor address register, a anchor address register, a common read/write address operator and at least two adders~~

a multiplexer sequentially providing a plurality of input values including at least one output of at least two adders and an address of a block to a next anchor address register;

a first adder of the at least two adders outputting a sum of a next anchor address of the next anchor address register and a line offset;

a second adder of the at least two adders outputting a difference of the next anchor address of the next anchor address register and a desired value;

an anchor address register receiving the next anchor address from the next anchor address register; and

a common read/write address operator operating upon the received next anchor address to generate the common read/write address;

reading image data of a block scan order from the common read/write address of the line memory;

storing image data of the raster scan order in the common read/write address of the line memory;

converting stored image data of raster scan order to the block scan order; and

transmitting image data of the block scan order to an encoder, the encoder encoding the received image data.

Claim 49: (Cancelled)

Election/Restrictions [Rejoinder]

8. Claims 1 and 32 [claims 3-18 are dependent upon claim 1 and claims 19-31 and 33-48 are dependent upon claim 32] are allowable. Claims 22-31, 37-42 and 44-47, previously withdrawn from consideration as a result of a restriction requirement, require all the limitations of an allowable claim. Pursuant to the procedures set forth in MPEP § 821.04(a), **the restriction requirement among inventions Species II-V, as set forth in the Office action mailed on 6/22/2007, is hereby withdrawn** and claims 22-31, 37-42 and 44-47 are hereby rejoined and fully examined for patentability under 37 CFR 1.104. In view of the withdrawal of the restriction requirement, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

REASONS FOR ALLOWANCE

9. The following is an examiner's statement of reasons for allowance:

Independent claims 1 and 32 are allowable over the prior art of record. Claims 3-18 depend from claim 1 respectively, therefore are allowed. Claims 19-31 and 33-48 are dependent upon claim 32 respectively, therefore are allowed.

Independent claim 1 recites the limitations of: a line memory for storing image data of a plurality of lines; an address generating block for converting supplied image data of raster scan order to block scan order by generating a common read/write address for the line memory so that only one line memory is required for performing simultaneous read and write operations, the address generating block including a block address generator for generating an address of a block which image data is read from and written into; a line offset generator for providing a line offset between an earlier common read/write address and a present common read/write address for the line memory; and an address generator including a multiplexer sequentially providing a plurality of input values including at least one output of at least two adders and the address of the block to a next anchor address register; a first adder of the at least two adders outputting a sum of a next anchor address of the next anchor address register and the line offset; a second adder of the at least two adders outputting a difference of the next anchor address of the next anchor address register and a desired value; an anchor address register receiving the next anchor address from the next anchor address register; and a common read/write address operator operating upon the received next anchor address to generate the common read/write address.

Independent claim 32 recites the limitations of: generating a common read/write address for a line memory of a plurality of lines for performing simultaneous read and write operations using an address generator having a multiplexer sequentially providing a plurality of input values including at least one output of at least two adders and an address of a block to a next anchor address register; a first adder of the at least two adders outputting a sum of a next anchor address of the next anchor address register and a line offset; a second adder of the at least two adders outputting a difference of the next anchor address of the next anchor address register and a desired value; an anchor address register receiving the next anchor address from the next anchor address register; and a common read/write address operator operating upon the received next anchor address to generate the common read/write address; reading image data of a block scan order from the common read/write address of the line memory; storing image data of the raster scan order in the common read/write address of the line memory; converting stored image data of raster scan order to the block scan order.

The combination of these features as cited in the claims in combination with the other limitations of the claims are neither disclosed nor suggested by the prior art of record.

The closest reference Rengakuji (US 6,212,300 B1) discloses block/raster conversion on color image data by reading and writing into a temporary memory. However, Rengakuji does not teach the limitations cited above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard Krasnic whose telephone number is (571) 270-1357. The examiner can normally be reached on Mon-Thur 8:00am-4:00pm and every other Friday 8:00am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on (571) 272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jingge Wu/
Supervisory Patent Examiner, Art Unit 2624
Bernard Krasnic

December 23, 2008